R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising a first circuit generally configured to wake-up a second circuit in response to an input signal. The input signal generally comprises a programmable delay value.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, FIGS. 1-3 and in the specification as originally filed, for example, on page 4, line 7 through page 5, line 14, on page 8, line 11 through page 9, line 18, on page 10, lines 4-17, on page 12, line 4 through page 13, line 6 and on page 16, line 1, page 17, line 6. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 4, 5 and 16 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 13 and 14 under 35 U.S.C. §102(b) as being anticipated by O'Brien et al. '205 (hereinafter O'Brien) is respectfully traversed and should be withdrawn.

O'Brien is directed to a power management control technique for timer tick activity within an interrupt driven computer system (Title). A timing unit 30 of O'Brien generates a timer tick interrupt signal at a predetermined (i.e., fixed) rate of 18.2 times per second (column 4, lines 10-15 of O'Brien). A wake-up period occurs in response to assertion of the timer tick interrupt signal (Abstract). Because the timer tick interrupt signal that starts the wake-up period has a fixed period, O'Brien does not disclose or suggest a first circuit configured to wake-up a second circuit in response to an input signal, where the input signal comprises a **programmable delay value**, as presently claimed.

In contrast, the presently claimed invention (claim 1) provides a first circuit configured to wake-up a second circuit in response to an input signal, where **the input signal comprises a programmable delay value**. Claims 14 and 15 include similar recitations. Because O'Brien does not disclose or suggest waking up a circuit in response to an input signal where the input signal comprises a programmable delay value, as presently claimed, O'Brien does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As

such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, assuming, *arguendo*, one skilled in the art would view (i) the power management unit (PMU) 10 of O'Brien as being similar to the presently claimed first circuit and (ii) the programming input 59 of O'Brien as being similar to the presently claimed input signal (as suggested on page 3, lines 1-3 of the Office Action and for which Applicant's representative does not necessarily agree), O'Brien does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. In particular, in response to a timer tick interrupt, the PMU 10 of O'Brien causes the CPU clock signal and the system clock signal to be driven at the maximum frequencies for a pre-programmed time period determined by a programmable counter 56 (see column 6, lines 23-53 of O'Brien). The programming input 59 is used to program the programmable counter 56 (column 6, lines 44-49 of O'Brien). When the transitory time period as determined by programmable counter 56 lapses, the frequencies of the CPU clock and system clock are reduced, i.e. a suspend or sleep mode is entered (see Abstract and column 6, lines 49-53 of O'Brien).

Since (i) the power management unit 10 of O'Brien causes the computer system to enter **a sleep state** (i.e., the CPU clock signal and the system clock signal to be driven at reduced frequencies) in response to the lapse of the delay set by the

programmable counter 56 and (ii) the delay of the programmable counter 56 is set by the programming input 59, it follows that O'Brien does not disclose or suggest a first circuit configured to **wake up** a second circuit in response to an input signal where the input signal comprises a programmable delay value, as presently claimed. Therefore, O'Brien does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, assuming, *arguendo*, one skilled in the art would view (i) the power management unit (PMU) 10 of O'Brien as being similar to the presently claimed first circuit and (ii) the timer tick interrupt of O'Brien as being similar to the presently claimed input signal (a position not addressed by the Office Action but which Applicant's representative addresses for completeness), O'Brien still does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. In particular, since (i) the power management unit 10 of O'Brien causes the CPU clock signal and the system clock signal to be driven at the maximum frequency (i.e., a wake-up state) in response to the timer tick interrupt (column 6, lines 27-38 of O'Brien) and (ii) the timer tick interrupt occurs 18.2 times per second, **regardless of other system activity** (column 2, lines 39-41

of O'Brien), it again follows that O'Brien does not disclose or suggest a first circuit configured to **wake up** a second circuit in response to an input signal where **the input signal comprises a programmable delay value**, as presently claimed. Therefore, O'Brien does not disclose or suggest each and every element of the presently claimed invention arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, since the timing unit 30 of O'Brien (i) does not receive an input (see FIG. 1 of O'Brien) and (ii) generates a timer tick interrupt signal at a predetermined (i.e., fixed) rate, regardless of other system activity (see column 2, lines 39-41 and column 4, lines 10-15 of O'Brien), one skilled in the art would not view the timing unit 30 as being the same as a first circuit configured to **wake up** a second circuit in response to **an input signal** where **the input signal comprises a programmable delay value**, as presently claimed. Therefore, O'Brien does not disclose or suggest each and every element of the presently claimed invention arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-13 and 16-20 depend, either directly or indirectly, from claim 1 or claim 15 which are believed to be allowable. New claims 21-25 depend, either directly or indirectly,

from claims 1, 14 or 15 and are believed to be fully patentable over the cited reference. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 6-12, 15 and 17-20 under 35 U.S.C. §103(a) as being unpatentable over O'Brien in view of MacDonald '328 (hereinafter MacDonald) is respectfully traversed and should be withdrawn.

The conclusory statements on page 4, lines 2-4 of the Office Action that "it would have been obvious to a person of ordinary skill in the art to apply the details as taught by MacDonald to the first circuit in the apparatus of O'Brien" and "the motivation for doing so would have been to ensure the integrity of the apparatus" do not adequately address the issue of motivation (see *In re Lee*, 61 USPQ2d 1430, 1434 (Fed.Cir. 2002)). The Federal Circuit has stated:

> This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher." *(See In re Lee* (brackets in original, citations omitted)).

The Office Action fails to present objective factual evidence or a convincing line of reasoning regarding the principle or understanding within the art that would have compelled one of ordinary skill in the art **with no knowledge of the present invention** to have selected, combined or modified the cited references (see page 4, lines 1-4 of the Office Action). Therefore, the Office Action fails to meet the Office's burden to factually establish a *prima facie* case of obviousness (MPEP §2142). As such, the presently claimed invention is fully patentable under 35 U.S.C. §103(a) and the rejection should be withdrawn.

Furthermore, even assuming, *arguendo*, the references were combinable (for which Applicant's representative does not necessarily agree), the combination of O'Brien and MacDonald as urged by the Office Action on page 4, lines 1-4 would appear to only teach **varying the length of a period that a circuit remains awake** after assertion of a timer tick interrupt occurs (see column 2, lines 64-67 of O'Brien). Neither O'Brien nor MacDonald appear to provide a suggestion or motivation to provide a programmable delay value or programmable period of time for waking up a circuit, as presently claimed. It is improper, in determining whether a person of ordinary skill would have been led to a combination of references, simply to "[use] that which the inventor taught against its teacher." (See In re Lee (citing W.L. Gore v. Garlock, Inc., 220 USPQ 303, 312-13)). Therefore, the Office Action fails to meet

the Office's burden to factually establish a *prima facie* case of obviousness (MPEP §2142). As such, the presently claimed invention is fully patentable under 35 U.S.C. §103(a) and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please replace the paragraph beginning at page 3, line 15 with the following paragraph:

Referring to FIG. 1, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. In one example, the circuit 100 may be implemented as a user programmable wake-up timer. The circuit 100 may implement a programmable wake-up timer that may be used with a processing device, such as a microprocessor or a microcontroller, to control the exiting of a suspend or sleep mode. The circuit 100 may also allow variations in the wake-up time (that may result from processing or operating conditions) to be tuned out. The circuit 100 may allow a user to program a delay value for a wake-up operation. The [timer] circuit 100 may have a low-power consumption and may operate in a low-power suspended state without requiring any additional pins or external components.

Please replace the paragraph beginning at page 4, line 7 with the following paragraph:

The circuit 100 may [be required to] provide a periodic wake-up indication. The circuit 100 may [be required to] provide

the periodic wake-up indication to allow a device (e.g., a computer) to respond to an event (e.g., push of a button or mouse movement). A timing of the wake-up indication may be programmed by a user. The circuit 100 may allow for significant variation and/or adjustment of the wake-up time for different users/applications. The circuit 100 may provide a reasonable accuracy in sleep time (e.g., efficient use of suspend mode power budget). In the example of a Universal Serial Bus (USB) microcontroller, an average current of less than 500 uA during suspend may be implemented. However, other suspend currents may be implemented accordingly to meet the design criteria of a particular implementation. Additionally, the circuit 100 may be configured to operate between two operating modes. For example, the circuit 100 may operate under any power conditions between a full operation mode and a sleep (or suspend) operation mode (e.g., between (i) a low speed/high speed mode, (ii) a low power/high power mode, etc.). The circuit 100 may eliminate pins previously used for external wake-up components.

Please replace the paragraph beginning at page 6, line 11 with the following paragraph:

In one example, the delay block 102 may be implemented as an analog delay circuit. In another example, the delay circuit 102 may be implemented as a current charging a capacitor, a ring

oscillator, and/or a R-C delay time. However, the delay block 102 may be implemented as other types delay devices in order to meet the criteria of a particular implementation. The delay circuit 102 may be implemented as a slow-charging circuit having minimal power consumption. The delay block 102 may be configured to provide a baseline delay time (e.g., the signal DELAY). The signal DELAY and, therefore, the delay time of the circuit 100 may typically have a wide variation in an integrated circuit application. The variation of the signal DELAY is generally dominated by silicon processing variations in the fabrication of the integrated circuit containing the circuit 100.

Please replace the paragraph beginning at page 12, line 4 with the following paragraph:

The wake-up time of the timer 100 may be tuned (e.g., programmed) by the signal ADJUST[3:1]. Additionally, the wake-up time for a device may be measured during a normal operation (e.g., non-suspended). The measurement of the wake-up time for a particular chip may be accomplished by (i) determining an initial wake-up setting, (ii) starting the wake-up timer 100 (which runs in either awake or suspended modes), (iii) determining a delay time between enabling the wake-up timer 100 and an assertion of the signal OUTPUT and (iv) changing the initial wake-up setting in

response to the delay time. The measured wake-up time may indicate a speed of the chip (under the current conditions). The timer 100 may allow a user and/or appropriate firmware to select the best wake-up setting for the particular chip. The wake-up setting may be stored in a register and presented [to] as the signal ADJUST[3:1] during suspend mode (if the circuit is enabled).

Please replace the paragraph beginning at page 14, line 1 with the following paragraph:

The delay circuit 102' may clock the counter 140. The delay counter 102' may clock the counter with the delay clock DELAY. An initial count of the counter 140 may be provided by the signal ADJUST[3:1]. The counter 140 may count UP/DOWN in response to the signal DELAY [and the signal ADJUST[3:1]]. The counter 140 may count from the initial value determined from the signal ADJUST[3:1]. The initial value of the signal ADJUST[3:1] may be programmed. Additionally, the initial value may be programmed by a user. When the counter 140 reaches a predetermine value determined by the signal ADJUST[3:1], the counter 140 may assert the signal OUTPUT. For example, the counter 140 may start from an initial value determined by the signal ADJUST[3:1] and count up/down to a target value (e.g., 0 or 7). Additionally, the counter 140 may start from an initial value (e.g., 0 or 8) and

count up/down to a target value determined by the signal ADJUST[3:1].

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus comprising:

a first circuit configured to [wake-up] wake up a second circuit in response to an input signal, wherein said input signal comprises a programmable delay value.

4. (AMENDED) The apparatus according to claim 1, wherein said [delay value comprises a] programmable delay value is determined by said apparatus in response to one or more firmware instructions.

5. (AMENDED) The apparatus according to claim 1, wherein said programmable delay value comprises a wake-up delay timing value.

6. (AMENDED) The apparatus according to claim 1, wherein said first circuit comprises:

a delay circuit configured to present a first delay signal; and

a select circuit configured to present a second delay signal in response to said first delay signal and said input signal, wherein said second delay signal is configured to [wake-up] wake up said second circuit.

8. (AMENDED) The apparatus according to claim 7, wherein said programmable delay comprises a multiple of a delay of said first delay signal.

9. (AMENDED) The apparatus according to claim 6, wherein said select circuit is further configured to select one of a plurality of third delay signals in response to said input signal.

11. (AMENDED) The apparatus according to claim 6, wherein said select circuit comprises a counter configured to generate said second delay signal in response to said input signal and said first delay signal.

12. (AMENDED) The apparatus according to claim 6, wherein said delay circuit is further configured to present said first delay signal in response to an enable signal.

14. (AMENDED) An apparatus comprising:

a first circuit configured to operate in a [first] sleep mode [or] and a [second] wake-up mode; and

a second circuit configured to control switching of said first circuit from said [first] sleep mode to said [second] wake-up mode after a programmable period of time.

15. (AMENDED) A method for wake-up timing comprising the steps of:

(A) receiving an input signal; and

(B) waking-up a circuit <u>after a delay time determined</u> in response to said input signal, wherein said input signal comprises a programmable delay value.

16. (AMENDED) The method according to claim 15, wherein said input signal comprises a user programmable signal and said <u>programmable</u> delay value comprises a [programmable delay] <u>wake-up timing</u> value .

17. (AMENDED) <u>The method according to claim 15, wherein said programmable delay value is determined in response to execution of one or more computer executable instructions stored in</u> a computer readable medium [containing instructions to execute the steps of claim 15].

18. (AMENDED) The method according to claim 15, wherein step (B) further comprises the sub-steps of:

(B-1) presenting a first delay signal; and

(B-2) presenting a second delay signal in response to said first delay signal and said programmable delay value, wherein said second delay signal is configured to wake-up said circuit.

19. (AMENDED) The method according to claim 18, wherein step (B) further comprises the sub-step of:

(B-3) controlling a programmable delay of said second delay signal in response to said programmable delay value.

20. (AMENDED) The method according to claim 15, further comprising the step of:

(C) generating said input signal in response to [input pins, data pins, microprocessor code, and/or firmware] a comparison of a measured wake-up delay to a predetermined wake-up delay.

Please add the following new claims:

21. (NEW) The apparatus according to claim 1, wherein said first and second circuits are implemented on a single integrated circuit.

22. (NEW) The apparatus according to claim 1, wherein (i) said first circuit is configured to periodically wake up said second circuit and (ii) a sleep period of said second circuit is determined by said programmable delay value.

23. (NEW) The apparatus according to claim 1, wherein said second circuit is configured to generate said input signal.

24. (NEW) The method according to claim 15, further comprising:

setting an initial value for said programmable delay value;

enabling a wake-up delay timer configured to generate a wake-up signal in response to said programmable delay value;

measuring a delay time of said wake-up timer; and

adjusting said programmable delay value in response to said measured delay time.

25. (NEW) The apparatus according to claim 14, wherein said second circuit is configured to determine said programmable period of time in response to an input signal comprising a programmable delay value.